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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
LEE, SHUN K	

ART UNIT	PAPER NUMBER
2878	

DATE MAILED: 12/08/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/833,363	BOIERIU ET AL.	
	Examiner	Art Unit	
	Shun Lee	2878	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 May 2003, 18 Aug 2003 & 20 Oct 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 August 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *0503 &1003*
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. The corrected or substitute drawings were received on 18 August 2003. These drawings are not acceptable. It should be noted that the drawings fails to comply with 37 CFR 1.84 because the substitute specification has not been entered.

Specification

2. The substitute specification filed 18 August 2003 has not been entered because it does not conform to 37 CFR 1.125(b) and (c) because: a substitute specification submitted under this section must be submitted in clean form without markings as to amended material (as one example, see last paragraph on pg. 21; it should be recognized that other markings within the substitute specification have not been listed).

3. The disclosure is objected to because of the following informalities:

(a) on pg. 1, related application number is missing (an application for a patent when filed may incorporate "essential material" by reference to (1) a U.S. patent, (2) a U.S. patent application publication, or (3) a pending U.S. application, subject to certain conditions, see MPEP §608.01(p); and the guidelines for situations where applicant is permitted to fill in a number for Application No. _____ left blank in the application as filed can be found in *In re Fouche*, 439 F.2d 1237, 169 USPQ 429 (CCPA 1971));

(b) on pg. 1, "carries" in line 10 should probably be --carriers--; and

(c) on pg. 8, "window 34" in line 6 should probably be --photodiode 34--.

Appropriate correction is required.

4. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

6. Claim 13 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The specification discloses (pg. 21, lines 4-11) that a concentrated NH_4F (20%-40%) is used. However, there was no disclosure of the composition of the concentrated NH_4F etchant. Further, the specification fails to disclose temperature at which the two-step etch process occur. Thus claim 13 contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Applicant argues that one skilled in the art could practice this etch step right away without any further information since ammonium fluoride is commonly available in 40% aqueous solution (Attachment E) and cites Attachment F and column 2, line 59 to column 3, line 6 of Kaganowicz *et al.* as support. Examiner respectfully disagrees. Cited Attachment

E simply indicates that ammonium fluoride 40% solution is commercially available. Cited Attachment E states that conventional and modified etchants comprise ammonium fluoride plus other ingredients each of which have different critical temperatures and etch rates. Further, Kaganowicz *et al.* state (column 2, line 59 to column 3) that "In accordance with the present invention, prior to deposition of the passivating layer, the surface of the semiconductor device is treated with an aqueous ammonium fluoride-hydrogen fluoride solution. Commonly known as buffered HF or ammonium bifluoride, this solution typically comprises from about 4:1 to about 6:1 ratio by volume of an aqueous solution containing about 40 percent by weight of ammonium fluoride and an aqueous solution containing about 49 percent by weight of hydrogen fluoride. Commercial standard buffered HF generally contains these solutions in a ratio by volume of about 5:1. The treatment is suitably carried out at room temperature for between about 15 and 100 seconds, which has been found is suitable for indium phosphide-based photodetectors, with about 30 seconds of treatment being preferred". Thus it is clear that the echant of Kaganowicz *et al.* comprise ammonium fluoride plus other ingredients. Therefore since there was no disclosure of the composition of the concentrated NH_4F etchant and the temperature at which the two-step etch process occur, the specification does not enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

9. Claims 1, 3, 6, 10, and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bevan *et al.* (US 5,838,053) in view of Tew *et al.* (US 4,686,373), Zanio *et al.* (US 4,910,154), and Goodwin (incorporated by reference US 5,300,777).

In regard to claim **10**, Bevan *et al.* (and US 5,300,777 which is incorporated by reference in lines 9 and 10 on column 5) disclose (Figs. 6-8) an infrared sensing device having at least one infrared light sensitive element (photodiode 30 or array 24; column 4, line 62 to column 5, line 7) comprising: a readout integrated circuit (20) formed at a face of a single-crystal silicon layer (12) having a tilt of approximately one degree from the (100) crystal direction (*i.e.*, nominal (100) lattice orientation; column 3, lines 9-12); at least one infrared light sensitive element (30 or 24) epitaxially grown on the face of the silicon layer (12), said at least one infrared light sensitive element (30 or 24) including:

(a) buffer layer (14a, 14b, 14c, 16) formed of a Group II - VI material including Cd and Te, the buffer layer (14a, 14b, 14c, 16) epitaxially grown on the silicon layer (12);

(b) a first layer (18a) of Group II-VI semiconductor material (*e.g.*, HgCdTe) epitaxially grown on said buffer layer (14a, 14b, 14c, 16), said first layer (18a) of Group II-VI semiconductor material including Hg, Cd and Te and having a first band gap;

(c) said buffer layer (14a, 14b, 14c, 16) functionally reducing mismatch (column 2, lines 22-29) between said silicon layer (12) and said first layer(18a) of Group II-VI semiconductor material;

(d) a second layer (18b) of Group II-VI semiconductor material including Hg, Cd and Te (*e.g.*, HgCdTe) epitaxially grown on said first layer (18a) of Group II-VI semiconductor material, said second layer (18b) of Group II-VI semiconductor material having a second band gap; and

(e) said first band gap being smaller than said second band gap (incorporated by reference US 5,300,777 column 2, line 62 to column 3, line 1).

The device of Bevan *et al.* lacks that the at least one infrared light sensitive element (30 or 24) is a mesa. However, infrared light sensitive element as a mesa is well known in the art. For example, Tew *et al.* teach (column 8, lines 44-51) that the infrared light sensitive element is a mesa (120 in Fig. 17). As another example, Zanio *et al.* teach (column 8, lines 44-51) that the infrared light sensitive element is a mesa (14 in Fig. 1 or 24 in Fig. 2) having a height of ~15 μm. As still another example, Goodwin teaches (column 4, lines 44-51) that the infrared light sensitive element is a mesa. Therefore it would have been obvious to one having ordinary skill in the art that the at least one

infrared light sensitive element in the device of Bevan *et al.* is a conventional mesa having a height of about 15 μm.

In regard to claim **11** which is dependent on claim 10, Bevan *et al.* also disclose (Figs. 6-8) a first cell and a second cell not overlapping the first cell (*i.e.*, an infrared detecting array of p-n junction diodes; column 4, line 62 to column 5, line 7) at least partially extending into said first layer of Group II-VI semiconductor material where first and second conductive interconnect traces (32 or equivalently 24 and 26; column 5, lines 46-48) are formed between the infrared detecting cells (30) and signal input gates of said readout circuit (20) and that the conductive interconnect traces monolithically connect the infrared detecting cells lying in one plane to the readout integrated circuits lying in another plane. The device of Bevan *et al.* lacks that the first and second conductive interconnect trace running over a first and second sloped side of the mesa, respectively. Tew *et al.* teach (column 8, lines 44-51; Fig. 17) that connection of n-type regions 114 of an active device mesa 120 to an aluminum pad on the silicon occurs through a via 122 located adjacent to the active device mesa 120. Therefore it would have been obvious to one having ordinary skill in the art to provide first and second conductive interconnect trace running over a first and second sloped side of a conventional mesa having a height of about 15 μm in the device of Bevan *et al.*, in order to connect first and second cells of the infrared detecting array to readout circuit signal input gates which are located adjacent to the mesa.

In regard to claims **1** and **3**, Bevan *et al.* in view of Tew *et al.*, Zanio *et al.*, and Goodwin is applied as in claim 11 above.

In regard to claim **6** which is dependent on claim 1, Bevan *et al.* in view of Tew *et al.* (US 4,686,373), Zanio *et al.*, and Goodwin is applied as in claim 11 above for rows of infrared detecting cells and rows of signal input gates of said readout circuit.

10. Claims 2 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bevan *et al.* (US 5,838,053) in view of Tew *et al.* (US 4,686,373), Zanio *et al.* (US 4,910,154), and Goodwin (incorporated by reference US 5,300,777) as applied to claim 1 above, and further in view of Chapman *et al.* (US 5,581,084).

In regard to claim **2** (which is dependent on claim 1) and claim **4** (which is dependent on claim 1), Bevan *et al.* in view of Tew *et al.*, Zanio *et al.*, and Goodwin is applied as in claim 11 above. The modified device of Bevan *et al.* lacks that the infrared detecting cell has a common contact which is conductively connected a common contact of the readout integrated circuit. Infrared detecting cells are well known in the art. For example, Chapman *et al.* teach (Fig. 6) that infrared detecting cells have a common anode contact which is conductively connected a common contact of the readout integrated circuit. Therefore it would have been obvious to one having ordinary skill in the art to connect the common anode contact of two color infrared detecting cells in the modified device of Bevan *et al.* to the readout integrated circuit, in order to detect infrared in two wavelength bands as taught by Chapman *et al.*

11. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bevan *et al.* (US 5,838,053) in view of Tew *et al.* (US 4,686,373), Zanio *et al.* (US 4,910,154), Goodwin (incorporated by reference US 5,300,777), and

Chapman *et al.* (US 5,581,084) as applied to claim 4 above, and further in view of Bean *et al.* (US 3,936,929).

In regard to claim **5** which is dependent on claim 4, the modified device of Bevan *et al.* lacks that a sloped side of said mesa has a slope angle between about 40 and 50 degrees relative to the mesa base. Mesas are well known structures. For example, Bean *et al.* teach (column 4, lines 16-30) mesas formed in (100) crystal orientation material have well known slopes of 46° or 54° and that metallic interconnects formed on these mesa slopes allow dependable electrical connection. Therefore it would have been obvious to one having ordinary skill in the art to provide a mesa slope angle between about 40 and 50 degrees in the modified device of Bevan *et al.*, in order to form dependable electrical connections as taught by Bean *et al.*

12. Claims 7-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bevan *et al.* (US 5,838,053) in view of Tew *et al.* (US 4,686,373), Zanio *et al.* (US 4,910,154), and Goodwin (incorporated by reference US 5,300,777) as applied to claim 6 above, and further in view of Koehler (US 4,137,544).

In regard to claims **7-9** which are dependent on claim 6, the modified device of Bevan *et al.* lacks that the infrared detecting cells include an arsenic compound at least partially extending into the first layer of Group II-VI semiconductor material wherein both the first and second layers of Group II-VI semiconductor material are formed of indium doped n-type HgCdTe. Infrared detecting cells are well known in the art. For example, Koehler teaches (Fig. 1) that the infrared detecting cells include an arsenic compound (14; column 3, lines 55-61) at least partially extending into the first layer (10) of Group

II-VI semiconductor material wherein both the first (10) and second (12) layers of Group II-VI semiconductor material are formed of n-type HgCdTe in order to provide an accumulation layer which prevents the natural inversion of n-type HgCdTe (column 4, lines 26-29). Koehler also teaches (column 4, lines 31-36) that n-type HgCdTe can be formed by ion implantation or diffusion of donor impurities such as indium. Therefore it would have been obvious to one having ordinary skill in the art to provide two layers of indium doped n-type HgCdTe and to form pn junction by implanting an arsenic compound in the modified device of Bevan *et al.*, in order achieve a desired detectivity in the 8-14 μm wavelength region as taught by Koehler (column 2, lines 53-60).

13. Claims 12 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bevan *et al.* (US 5,838,053) in view of Goodwin (incorporated by reference US 5,300,777), de Lyon (US 5,306,386), Kub *et al.* (US 6,242,324), and Wu *et al.* (US 6,043,141).

In regard to claims **12** and **16**, Bevan *et al.* is applied as in claims 10 and 11 above. The method of Bevan *et al.* lacks inserting a wafer with a read-out integrated circuit having a dihydride terminated passivating layer on the Si (001) surface (*i.e.*, dihydride terminated smooth surface by etching) into an MBE chamber and thermally cleaning at a temperature at or below 500°C to remove the passivating layer, then depositing the buffer layer, first layer, and the second layer in sequence on the Si (001) surface while maintaining the read-out integrated circuit at a temperature less than 500°C. MBE is well known in the art. For example, Bevan *et al.* teach (column 1, lines 10-61) it is known in the art to deposit a CdTe buffer layer and a HgCdTe layer on a Si

(001) surface by MBE. As another example, de Lyon teaches (column 3, line 54 to column 4, line 54) to deposit a CdTe buffer layer and a plurality of layers on a Si (001) surface by MBE. As still another example, Kub *et al.* teach (column 8, lines 48-52) the typical way preparing a silicon surface that is free of oxide prior to epitaxial growth is to hydrogen terminate (*i.e.*, dihydride terminated) the silicon surface and then desorb the hydrogen in vacuum at temperatures of approximately 500°C. As a further another example, Wu *et al.* teach (column 5, lines 60-67) to deposit HgCdTe layers on a semiconductor surface by the MBE (which is the typical method of in situ growth of high quality HgCdTe epilayers having abrupt heterojunctions in a single growth run; column 1, lines 19-31) at a temperature less than 500°C preferably in a range of 155 to 165°C. Therefore it would have been obvious to one having ordinary skill in the art to thermally clean at ~500°C and MBE deposit a CdTe buffer layer followed by first and second HgCdTe layers on a Si (001) surface at a temperature less than 500°C in the method of Bevan *et al.*, in order obtain abrupt heterojunctions in a single growth run.

14. Claims 13-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bevan *et al.* (US 5,838,053) in view of Goodwin (incorporated by reference US 5,300,777), de Lyon (US 5,306,386), Kub *et al.* (US 6,242,324), and Wu *et al.* (US 6,043,141) as applied to claim 12 above, and further in view of La Chapelle, Jr. (US 5,366,934), McConnell *et al.* (US 4,778,532), Hetrick *et al.* (US 6,096,149), Kaganowicz *et al.* (US 4,705,760), Norimatsu *et al.* (US 6,049,638), Tew *et al.* (US 4,686,373), and Koehler (US 4,137,544).

In regard to claims **13-15** which are dependent on claim 12, the method of Bevan *et al.* lacks a detailed description of the semiconductor process techniques (*i.e.*, removing a passivation layer by etching with a diluted solution of $HF:H_2O$ and forming the dihydride terminated smooth Si(001) surface by etching with a concentrated solution of NH_4F; depositing a thin CdTe cap layer on the second HgCdTe layer; coating the entire structure with a photoresist; selectively opening a plurality of windows in the photoresist; fabricating a plurality of p-n junctions by implementing arsenic atoms through the windows selectively by ion implantation technique; annealing the ROIC to activate the arsenic; removing the masking photoresist layer; selectively protecting the grown infrared material structure with a photoresist while leaving the remaining areas uncovered; etching the uncovered areas to expose the ROIC contact pads; selectively protecting the grown infrared material structure with a photoresist, leaving the rest of the areas open; and forming a 40-50° side wall slope mesa structure by etching with an etching solution such as 4% bromine in hydrobromic acid solution) used to fabricate the infrared sensing device. However, semiconductor process techniques such as passivation layers, photoresist masks, selective etching, and selective ion implantation are well known in the art. For example, La Chapelle, Jr. teaches (column 1, lines 18-66) it is well known in the art to provide a passivation layer in order to enhance and preserve the best detector properties. As another example, McConnell *et al.* teach (column 5, line 39 to column 6, line 14) etchants comprising HF are well known in the art; Hetrick *et al.* (column 1, line 64 to column 2, line 2) and Kaganowicz *et al.* (column 2, lines 59-68) teach etchants comprising NH_4F are well known in the art; and

Norimatsu *et al.* teach (column 4, lines 56-63) that wet etching can be performed with an etchant comprising bromine in hydrobromic acid. As still another example, Tew *et al.* teach (column 5, lines 21-33) to provide a photoresist mask for selective etching and Koehler teaches (column 3, lines 43-61) to provide a mask for selective ion implantation. Therefore it would have been obvious to one having ordinary skill in the art to use standard semiconductor processing techniques in the modified method Bevan *et al.* in order to form the infrared sensing device.

Response to Arguments

15. Applicant's arguments filed 18 August 2003 have been fully considered but they are not persuasive.

In response to applicant's arguments (second paragraph on pg. 14 to first paragraph on pg. 17 of remarks filed 18 August 2003) against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

In response to applicant's argument (last paragraph on pg. 17 of remarks filed 18 August 2003) that Chapman *et al.* does not show an interconnect of any kind from a II-VI mesa to an ROIC formed at the face of a silicon layer on which the mesa had been epitaxially grown, the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the

references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981).

In response to applicant's arguments (first paragraph on pg. 18 of remarks filed 18 August 2003) against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). In this case, Bean *et al.* was cited as an example that mesas formed in (100) crystal orientation material have well known slopes of 46° or 54° and that metallic interconnects formed on these mesa slopes allow dependable electrical connection.

In response to applicant's arguments (last paragraph on pg. 18 of remarks filed 18 August 2003) against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Applicant's arguments (first paragraph on pg. 19 to fourth paragraph on pg. 21 of remarks filed 18 August 2003) with respect to amended claim 12 (with dependent claims 13-15) and newly added claim 16 have been considered but are moot in view of the new ground(s) of rejection. Also in response to applicant's argument that the examiner has combined an excessive number of references, reliance on a large number of references in a rejection does not, without more, weigh against the obviousness of

the claimed invention. See *In re Gorman*, 933 F.2d 982, 18 USPQ2d 1885 (Fed. Cir. 1991). Further in response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Conclusion

16. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shun Lee whose telephone number is (703) 308-4860. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Porta can be reached on (703) 308-4852. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

SL
November 26, 2003

DAVID PORTA
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800